

In the claims:

1. (Cancelled)
2. (Currently Amended) A method for analyzing an integrated circuit (IC) under test and for identifying and inserting test points in order to improve the testability of the IC, the method comprising:
 - a) determining a measure of testability for the IC;
 - b) selecting test point candidates to be evaluated for insertion in said IC and arranging said test point candidates into a first plurality of pairs of sets;
 - c) evaluating said first plurality of pairs of sets and forming a second plurality of pairs of sets from said first plurality of pairs of sets, said evaluation being based on the respective testability improvement achieved by each plurality of said pairs of sets, and recombining said first and second plurality of pairs of sets based on results from said evaluation;
 - d) repeating step c) until said first and second pairs of sets converge to form a best set, said best set providing the test points to be inserted into the IC; and
 - e) repeating steps a) through d) until all the test points to be inserted have been incorporated into the IC,

The method as recited in claim 1, wherein in step a) the measure of testability for the IC is determined by a combination of fault simulation and fault detection probability of detection calculations.
3. (Currently Amended) The method as recited in claim 2, further comprising including the steps of:

- a) performing a fault simulation using a set of random patterns to identify faults detected by the random patterns;
- bg) computing a measure of controllability based on the number of times the IC takes a predetermined logic value during the fault simulation;
- eh) deriving a measure of observability from the measure of controllability;
- di) assigning a detection probability of 1.0 to a fault that was detected by the random patterns;
- ej) assigning a detection probability for the remaining faults according to the measure of controllability and observability respectively derived from steps bg) and eh); and
- fk) accumulating the detection probability for all the faults in the IC.

4. (Currently Amended) The method as recited in claim 3, wherein in step bg) further comprises applying a first selection criteria, wherein said applying a first selection criteria comprises ~~the steps of~~:

- al) estimating the testability improvement of the IC derived from inserting the test point based on changes in the measure of controllability and observability;
- bm) measuring the number of faults having a probability of detection nearing 1.0 if an observable point is placed at a particular location in the IC; and
- en) determining cluster roots representing nodes having poor output controllability and good input controllability and using inputs of the cluster roots as candidate test points to be inserted in the IC.

5. (Currently Amended) The method as recited in claim 4 wherein in step en) the number of

candidate test points is computed as a linear function of the number of gates in the IC until a maximum number of candidate test points is reached..

6. (Currently Amended) A method for analyzing an integrated circuit (IC) comprising sequential and combinational logic gates under test and for identifying and inserting potential test points in order to improve the testability of the IC, the method comprising ~~the steps of~~:

- a) determining a first measure of testability for the IC;
- b) forming a plurality of first sets of test points and determining the size and the number of said plurality of first sets;
- c) evaluating the improvement in the testability of the IC in the presence of said plurality of first sets of test points;
- d) performing an inversion and a mutation of said plurality of first sets of test points;
- e) intermingling pairs of said first plurality of sets to form a second plurality of pairs of sets with said intermingled pairs of said first plurality of sets;
- f) evaluating said first plurality of pairs of sets and said second plurality of pairs of sets to select which first and second pairs of sets should be kept, said selected pairs of sets of said first and second plurality replacing the original first plurality of pairs of sets; ~~and~~
- g) determining a second measure of testability for the IC; and
- gh) comparing the first measure of testability for the IC to the second measure of testability to determine whether the selected plurality of first and second pairs of sets converges towards an optimal set to be inserted in the IC as additional test points.

7. (Original) The method as recited in claim 6, wherein in step b) the size of the sets of test points is determined as a linear function of the number of gates forming the IC and the number of the sets of test points thus far inserted, wherein the size of the sets of test points is limited by an arbitrary upper limit, said limit being increased as more sets of test points are inserted into the IC, and wherein the number of the sets is determined by dividing the number of test points by the size of the set.

8. (Currently Amended) The method of recited in claim 6, wherein in step c) said sets of test points are grouped into a plurality of first sets according to a predetermined selection criteria.

9. Cancelled.

10. (Currently Amended) The method as recited in claim 6 wherein in step d), performing an inversion and a mutation of said plurality of first sets of test points further comprises ~~the steps~~ of:

a) randomly selecting a starting point and an ending point for the inversion;
b) reversing all the points located between said the starting point and the ending point thereby interchanging said starting point with said ending point and all the points therebetween; and

e) selecting a mutation point and a random number to determine if mutation is to occur, wherein if said mutation occurs, the test point at the mutation point is arbitrarily replaced with another test point chosen at random from among the set of test points.

11. (Currently Amended) The method as recited in claim 6 wherein step e) further comprises pairing said sets of test points, wherein said pairing comprising ~~the steps of~~:

a1) selecting at random a first set of test points from said first plurality of sets;
b1) selecting at random a second set of test points from said first plurality of sets;
e1) selecting for the first member of the pair the set of test points from steps a1) or b1), according to which set has a higher testability;
d1) repeating steps a1) through e1) to select the second member of said pair;
e2) forming iteratively subsequent pairs as in steps a1) through d1); and
f1) repeating steps a1) through e2) until the pairs forming said first plurality have been selected.

12. (Currently Amended) The method as recited in claim ~~12~~ 11, further comprising the step of refreshing said first plurality of sets of test points to its original state and repeating steps a1) through f1) to generate a total number of pairs of test point sets to be intermingled.

13. (Currently Amended) The method as recited in claim 6 wherein in step d2) said intermingling comprises ~~the steps of~~:

a2) selecting at random a crossover starting point and ending point for each pair of sets (X and Y) to be intermingled;
b2) creating a first new set consisting of all the test points in (X) that reside within the starting and the ending points and of all test points in (Y) that are outside the starting and ending points; and
e2) creating a second new set consisting of all the test points in (X) that reside outside the

crossover starting and ending points and consisting of all test points in (Y) that are inside the crossover starting and ending points, said first and second new sets forming a pair of new sets.

14. (Original) The method as recited in claim 13 further comprises determining if the pair of new sets should be kept as part of ~~the a~~ population by determining if the testability of either set of the new pair of sets is better than the best testability achieved by either set of the original pair of sets; and else, removing the new pair of sets from the set of the original pair of sets from the population.

15. (Currently Amended) The method as recited in claim 6, wherein in step ~~gh~~), determining whether ~~the a~~ population of pairs of sets of test points has converged ~~when comparing the respective testability of the individual sets~~, and determining whether the convergence criteria have been met.

16. (Original) The method as recited in claim 6, wherein a plurality of sets of test points are processed in parallel on a plurality of computer processors to reduce the time required to perform the test point insertion process.

17. (Currently Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for analyzing an integrated circuit (IC) under test and for identifying and inserting test points in order to improve the testability of the IC, ~~said method steps~~ comprising:

- a) determining a measure of testability for the IC;

b) selecting test point candidates to be evaluated for insertion in said IC and arranging said test point candidates into a first plurality of pairs of sets;

c) evaluating said first plurality of pairs of sets and forming a second plurality of pairs of sets from said first plurality of pairs of sets, said evaluation being based on the respective testability improvement achieved by each plurality of said pairs of sets, and recombining said first and second plurality of pairs of sets based on results from said evaluation;

d) repeating step c) until said first and second pairs of sets converge to form a best set, said best set providing the test points to be inserted into the IC; and

e) repeating steps a) through d) until all the test points to be inserted have been incorporated into the IC,

wherein in step a) the measure of testability for the IC is determined by a combination of fault simulation and fault detection probability.